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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/066,171
Filing Date: February 01, 2002
Appellant(s): BEAMAN ET AL.

Dr. Daniel P. Morris
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed July 24, 2009 appealing from the Office action mailed November 26, 2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 49, 66, 81, 86, 88, 90-94 and 96.

Claims 50-60, 67-80, 82-85, 87, 89, 95 and 97-102 have been withdrawn from consideration as not directed to the elected species.

Claims 1-48 and 61-65 have been canceled.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

A substantially correct copy of the appealed claims appears on pages 9-17of the Appendix to the appellant's brief. The minor errors are as follows: Claim 94 had been amended in the paper filed on August 17, 2006. The Appendix does not show claim 94 as amended. The correct copy of claim 94 is as follows:

94. (Previously Presented) A method according to claim 49 comprising:

holding said substrate, for retractably moving said substrate towards and away from an electronic device so that said second ends contact electrical contact locations on said electronic device, and applying electrical signals to said elongated electrical conductors.

(8) Evidence Relied Upon

5,233,011	Saruwatari et al	8-1993
5,665,610	Nakata et al	9-1997
6,110,823	Eldridge et al	8-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112

Claims 92 and 93 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 92 as written is dependent on itself and, consequently, is *prima facie* indefinite. Claim 93 is dependent on claim 92.

Claim Rejections - 35 USC § 102

Independent claim 49 is rejected under 35 U.S.C. 102(e) as being anticipated by Eldridge et al (US 6,110,823).

The Eldridge et al patent (hereinafter Eldridge) is directed to a method for forming contact structures. The contact structures are formed by bonding a free end of a wire to a substrate, and subsequently overcoating the wire with a least one layer of material. See the abstract. The contact structures of Eldridge may be used as probes (column 14, lines 25-32). Thus, Eldridge is directed to the same field of endeavor as applicant's invention which, as indicated in the title, is directed to methods of fabrication of probe structures.

Figure 10k of Eldridge illustrates one of the several disclosed embodiments. One end 1086a of a wire having a first end and a second end is bonded to a surface of substrate 1076 (column 67, lines 45-50). This corresponds to the "providing" and "bonding" steps of claim 49. The wire stem 1086 is provided with a multi-layer coating. The coating process includes

application of a layer of dielectric material 1094 (column 67, lines 55-59). This corresponds to the "forming a dielectric coating" step of claim 49. Eldridge et al additionally disclose that a layer of conductive material (1096) is then deposited over the coated wire (column 67, lines 62-67). As indicated in the abstract and column 1, lines 26-42, the method is for forming a plurality of connections. All limitations recited in claim 49 are taught by Eldridge et al.

Dependent claims 81, 90, 91 and 96 are also rejected under 35 U.S.C. 102(e) as being anticipated by Eldridge et al (US 6,110,823).

With respect to claim 81, Eldridge et al shows in figure 10k that the conductor has a shape which is partially curved and partially linear.

With respect to claim 90, Eldridge et al discloses a resilient and/or compliant (springy) contact structure which is securely mounted to an electronic component, and which may be used for effecting temporary connection of the electronic component to another electronic component (column 12, lines 43-47). The resilient contact structures can be used to temporarily connect an electronic component for procedures such as burn-in and testing of the electronic component (column 14, lines 44-47).

With respect to claim 91, Eldridge et al discloses that it is known to utilize a test device with a plurality of wires in high density PCB and IC (integrated circuit) testing applications (column 5, lines 1-11).

With respect to claim 96, figure 5 of Eldridge et al shows conductor 502 with first end 502a bonded to a terminal 512 on substrate 508. The second end is formed with ball (protuberance) 534. See column 46, lines 55-62. Figure 5 shows conductor 502 coated with

inner coating layer 520 and outer coating layer 522. Eldridge teaches that the outermost (top) layer or both layers is/are a conductive material (column 47, lines 15-18; lines 38-39). This clearly indicates that the inner layer may be other than a conductive material, i.e., a dielectric material.

Claim Rejections - 35 USC § 103

Claim 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge et al (US 6,110,823) in view of Saruwatari et al (US 5,233,011).

Claim 66 differs from Eldridge et al by reciting specific materials from which the dielectric layer is formed. The Saruwatari et al patent is directed to a process for preparing an insulated wire. The insulation is made from a polyimide. See the abstract. Aromatic polyimide has excellent mechanical properties, solvent resistance, electrical insulative properties, and the highest thermal resistance among organic polymers. See column 1, lines 18-22. The prior art of record is indicative of the level of skill of one of ordinary skill in the art. It would have been obvious at the time the invention was made to have formed the dielectric insulation around the conductors of Eldridge from polyimide because polyimide has excellent mechanical and electrical properties as taught by Saruwatari et al.

Claims 86, 88 and 94 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge et al (US 6,110,823) in view of Nakata et al (US 5,665,610).

Eldridge et al recognizes that modern integrated circuits are generally produced by creating several, typically identical, integrated circuit dies on a single semiconductor wafer

(column 73, lines 1-4). "Burn-in" is a process whereby a chip (die) is either simply powered up or is powered up and signals exercising to some degree the functionality of the chip are applied. It is known to perform burn-in prior to singulating the dies. Typically, the temporary connections to the dies are made by test probes or by "flying wires". See column 73, lines 15-26.

Claim 86 differs from Eldridge et al by reciting that the plurality of conductors are distributed into a plurality of groups, while claim 88 recites that the groups are arranged in an array. The Nakata et al patent is directed to a semiconductor device checking method. Nakata et al teach that in order to guarantee the quality of bare (unpackaged) chips, it is necessary to perform checks such as burn-in while the device is part of the wafer. Nakata et al recognize that it takes a long time to check a plurality of bare chips formed on the wafer one by one. Consequently, it is required that a check such as burn-in should be made on a plurality, for example, 1000 or more bare chips while the chips are part of the wafer. A supply voltage and a signal to the check electrodes of a plurality of semiconductor chips formed on the wafer are simultaneously applied so as to operate the chips. It is necessary to prepare a probe card having a large number of probe terminals. See column 1, lines 27-46. Figure 3 shows an example of a semiconductor wafer housing for causing bump15 of the contactor 14 to come in contact with the check electrode 11 of the semiconductor chip 10. See column 5, lines 41-44. As illustrated in figure 3(a) and 3(b), bumps 15 are distributed in a plurality of groups of four which form an array. It would have been obvious at the time the invention was made to have formed the plurality of conductors in Eldridge into an array of groups as illustrated by Nakata et al because it would have facilitated testing each chip of a plurality of chips on a single wafer.

Claim 94 recites holding the substrate for retractably moving the substrate toward an electronic device and applying electrical signals to the conductors. Nakata et al disclose that in figures 3(a) and 3(b) element 21 is a holding plate for holding semiconductor wafer A. As shown in the figures, contactor 14 is adapted to be brought into contact with wafer A. See column 5, lines 45-54. As noted above, signals are supplied to the check electrodes so as to operate the chips. It would have been obvious at the time the invention was made to have provided a housing for retractably moving the substrate toward the conductors of Eldridge in a testing procedure as taught by Nakata et al because temporary contact with the wafer being tested would have been obtained.

(10) Response to Argument

At page 5 of the Brief, appellant states that "Eldridge et al. is not prior art under 35 USC 102 as described below." At the bottom of page 6 appellant argues that Eldridge at column 67, lines 55-59 provides no teaching of how the dielectric material can be applied over the nickel layer 1092. Appellant states that there is no enablement for this process and, consequently, no enablement for the structure of Eldridge figure 10k. At page 7 appellant argues that the Examiner has not made out a prima facie case showing that Eldridge is prior art under 35 U.S.C. 102.

These arguments are similar to appellant's arguments filed on February 24, 2009, after the final rejection of the claims. The advisory action mailed on March 20, 2009, referred to MPEP 2121 I. This section of the MPEP reads as follows in its entirety:

I. PRIOR ART IS PRESUMED TO BE OPERABLE/ENABLING

When the reference relied on expressly anticipates or makes obvious all of the elements of the claimed invention, the reference is presumed to be operable. Once such a reference is found, the burden is on applicant to provide facts rebutting the presumption of operability. In re Sasse, 629 F.2d 675, 207 USPQ 107 (CCPA 1980). See also MPEP § 716.07.

At page 8 of the Brief, appellant argues "The Examiner states '[a]s stated in MPEP 2121 1, prior art is presumed to be operable/enabling.' This is incorrect. The Examiner does not identify what part of MPEP 2121 1 supports this assertion. There is in fact none." Appellant further argues "The examiner states; 'The burden is on applicant to provide facts rebutting the presumption of operability.' The Examiner does not identify what part of MPEP 2121 1 supports this assertion. There is in fact none."

These arguments of appellant are in error. The title of MPEP 2121 I clearly states that the prior art is presumed to be operable/enabling. The second sentence of this section clearly states that the burden is on applicant. Appellant has provided no evidence that would rebut the presumption of operability of the Eldridge patent. Consequently, appellant's argument that Eldridge is not prior art is unpersuasive.

At page 7 of the Brief, appellant refers to section 2121.01 of the MPEP which appears immediately after section 2121 I. This section deals with prior art in rejections where operability in is question. Before addressing appellant's argument, the Examiner again observes that appellant has presented no evidence that would suggest that operability is in question. For the

sake of argument, if operability were considered to be in question, it is noted appellant emphasizes the statement in MPEP 2121.01 that "mere naming or description of the subject matter is insufficient, if it cannot be produced without undue experimentation." Appellant argues that "Since Eldridge provides no description of how to make the structure of Eldridge Fig. 10k, it is insufficient "mere naming or description of the subject matter." It is the Examiner's position that even if operability were in question, this argument is not convincing because appellant does not address the issue of undue experimentation. While mere naming or description of the subject matter is insufficient if it *cannot* be produced without undue experimentation, conversely it is sufficient if the subject matter *can* be produced without undue experimentation.

Section 2164.01 of the MPEP is entitled "Test of Enablement". This section the MPEP quotes *United States v. Telectronics, Inc*., 8 USPQ2d 1217, 1223 (Fed. Cir. 1998) "The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation." MPEP 2164.01 further states that "A patent need not teach, and preferably omits, what is well known in the art." It is the Examiner's position that processes of coating are well known in the art, do not require undue experimentation and, consequently, that it is not necessary for Eldridge to provide a description of that which is well known in order to be an enabling reference. One indication that coating processes are well known is the discussion of the prior art in the "Background of the Invention" section of the Eldridge patent. At column 3, lines 9-10 Eldridge state "it is known to coat bond wired and their surrounding connections (to the die and to a leadframe, e.g.) and refers to U.S. Pat No. 4,821,148. The Saruwatari et al patent, of

record, is also indicative of the level of skill in the art and shows that processes for coating wire with a dielectric are known in the art. Thus, even if the operability of Eldridge were in question, appellant's arguments would not be persuasive because Eldridge contains sufficient teaching to enable one of ordinary skill in the art to practice the invention without undue experimentation.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/William Leader/

Conferees:

/Patrick Ryan/

/William Krynski/